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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/005,489	STRASSER, ERICH	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-20* is/are allowed.

6)☒ Claim(s) *1-11,13 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bielski et al. (U.S. Pat. No. 6353397 B1) in view of Yoshiyuki (JP 9091045, English translation).

Bielski et al. teach a position measuring device for determining the position of two elements, which are movable with respect to each other (col. 2, line 66 to col. 3, line 15), comprising: a voltage source (fig. 1; col. 4, lines 37-46); and a scanning unit (fig. 1; col. 3, lines 1-3) comprising: one or more individual electrical components (fig. 1). Bielski et al. further teach: said position measuring device further comprises: an evaluation unit (fig. 1; and col. 3, lines 7-10); an interface by which said scanning unit transmits data to said evaluation unit, wherein said interface is not one of said one or more individual electrical components (fig. 1; and col. 4, lines 2-7); a graduation that moves relative to said scanning unit (col. 3, lines 1-3 and lines 16-20); said scanning unit further comprises a reading head that reads said graduation and generates position data that is sent to a position calculating unit that generates said data transmitted to

said evaluation unit (fig. 1; col. 3, lines 10-15 and lines 25-41); said reading head comprises a light source (col. 3, lines 25-41).

Bielski et al. do not mention explicitly a voltage monitoring unit that selectively supplies said one or more individual electrical components with a voltage from said voltage source based on a calculation of an internal resistance of said voltage source.

Yoshiyuki discloses a power supply voltage monitoring device, and teaches a voltage monitoring unit that selectively supplies said one or more individual electrical components with a voltage from said voltage source based on a calculation of an internal resistance of said voltage source (see the Abstract and the entire English translation of the detailed description of the invention).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Yoshiyuki in the Bielski position measuring device in order to provide an electronic device to be a load with an intelligent power supply which can protect said device from being damaged and malfunctioned when the input power supply voltage abnormally falls (Yoshiyuki, Abstract).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bielski et al. (U.S. Pat. No. 6353397 B1) in view of Yoshiyuki, as applied to claims 1 and 2 above, and further in view of Potega (U.S. Pat. No. 6459175).

Bielski et al. and Yoshiyuki teach a device that includes the subject matter discussed above. Bielski et al. and Yoshiyuki do not mention explicitly: said interface is a serial interface.

Potega teaches a serial connection with an A/D converter (col. 54, lines 47-67 and col. 55, lines 1-3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Potega serial interface in the Bielski and Yoshiyuki position measuring device in order to provide a digital data I/O with better communication opportunities (Potega, col. 54, lines 47-67 and col. 55, lines 1-3).

4. Claims 7–11, 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bielski et al. in view of Yoshiyuki, as applied to claim 1 above, and further in view of Hoon (U.S. Pat. No. 6104221).

Bielski et al. and Yoshiyuki teach a device that includes the subject matter discussed above. Bielski et al. and Yoshiyuki do not mention explicitly: said voltage monitoring unit monitors a supply voltage available to said one or more individual electrical components at a first time; said scanning unit further comprising a load connected to said voltage monitoring unit, wherein said voltage monitoring unit connects said load to said scanning unit at a second time and said voltage monitoring unit connects said voltage monitoring unit monitors a second supply voltage available to said one or more individual electrical components and said load at said second time. Bielski et al. and Yoshiyuki also do not teach: a method for the start-up of a position measuring device comprising a scanning unit, the method comprising: switching on a position measuring device that comprises a scanning unit; subsequent to said switching on, performing a check of a supply voltage of said scanning unit supplied by a voltage source; and activating one or more electrical components in said scanning unit,

provided a sufficient supply voltage for said activating has been determined during said performing said check; said performing said check comprises: measuring a supply voltage of said scanning unit for a first time; providing a defined load with a voltage; and calculating an internal resistance of said voltage source.

Hoon discloses a power-up detection circuit of a semiconductor device, and teaches: a voltage level detection unit which monitors a supply voltage available to said one or more individual internal circuits at a first time (col. 2, lines 1-30, lines 61-67 and col. 3, lines 1-5); a load connected to said voltage level detection unit, wherein said voltage level detection unit connects said load to said power-up detection circuit at a second time and said voltage level detection unit monitors a second supply voltage available to said one or more individual internal circuits and said load at said second time (col. 3, lines 54-67; col. 4, lines 1-3 and lines 37-59).

Hoon further teaches a method for the start-up of a semiconductor device (see Abstract), comprising: switching on a semiconductor device; subsequent to said switching on, performing a check of a supply voltage; and activating one or more internal circuits, provided a sufficient supply voltage for said activating has been determined during said performing said check (col. 1, lines 12-24; col. 2, lines 30; and col. 2, line 61 to col. 3, line 5). Hoon further teaches: said performing said check comprises: measuring a supply voltage for a first time; providing a defined load with a voltage; and calculating an internal resistance of said voltage source (col. 3, line 54 to col. 4, line 3; and col. 4, lines 37-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Hoon power-up detection circuit and method for the start-up of a semiconductor device in the Bielski and Yoshiyuki position measuring device in order to provide a stable voltage source for switching on and operating the said scanning unit (Hoon, col. 1, lines 12-33).

Allowable Subject Matter

5. Claims 14-20 are allowed.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claims 14-20 is the inclusion of the method step of measuring a second supply voltage of said scanning unit at a second time, wherein said calculating said internal resistance is based on said supply voltage of said scanning unit measured at said first time, said second supply voltage and a current consumption of said defined load. It is this step found in each of the claims, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant's arguments filed 05/28/2003 with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1-11, 13 and 21 are rejected as new art (JP 9091045 to Yoshiyuki) has been found to teach: a voltage monitoring unit that selectively supplies said one or more individual electrical components with a voltage from said voltage source based on a calculation of an internal resistance of said voltage source. For detailed response, please refer to section 2 set forth above in this Office Action.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (703)305-3467. The examiner can normally be reached on 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (703)308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

XS
XS
January 30, 2004

John Barlow
Supervisory Patent Examiner
Technology Center 2800